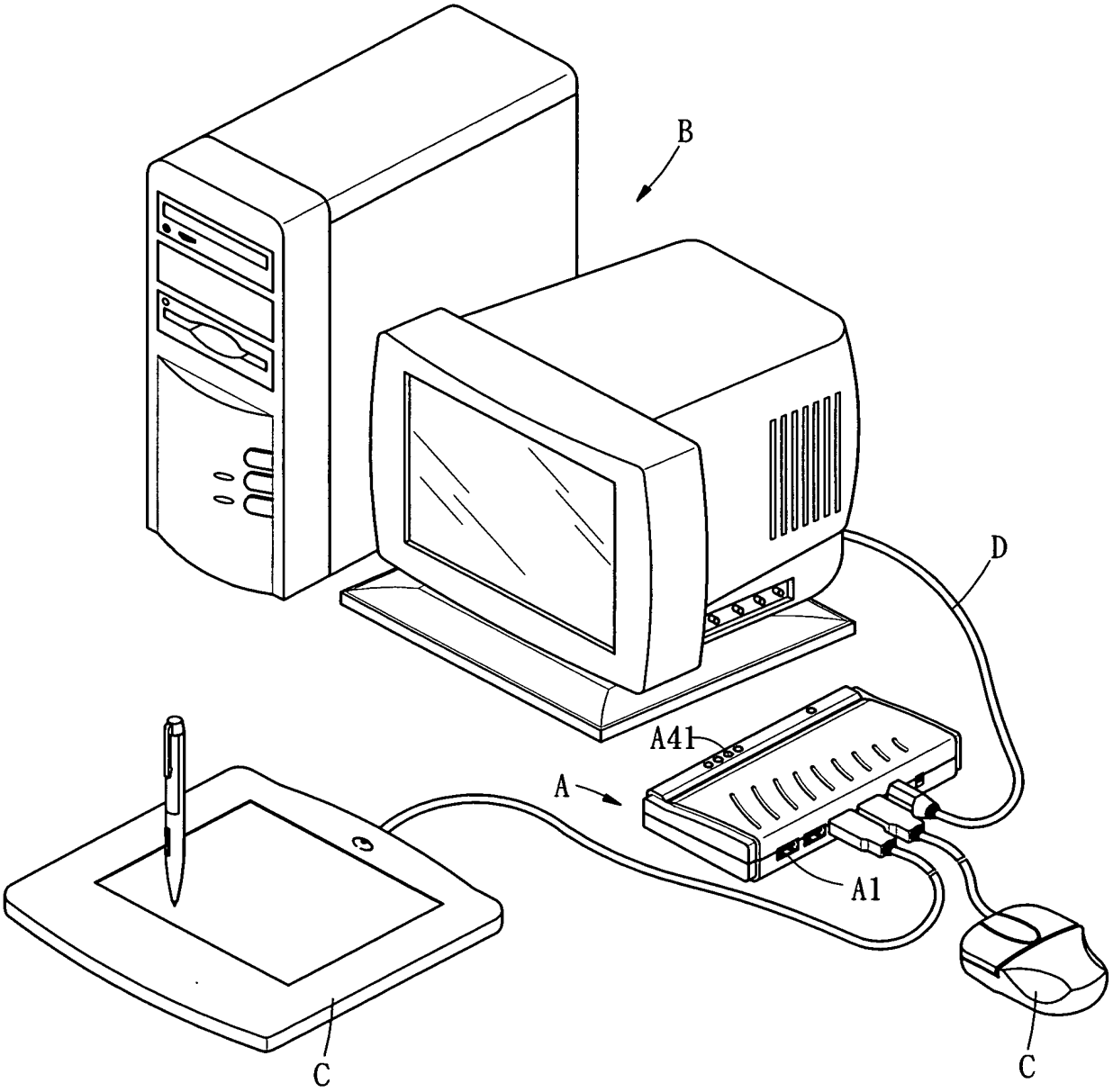
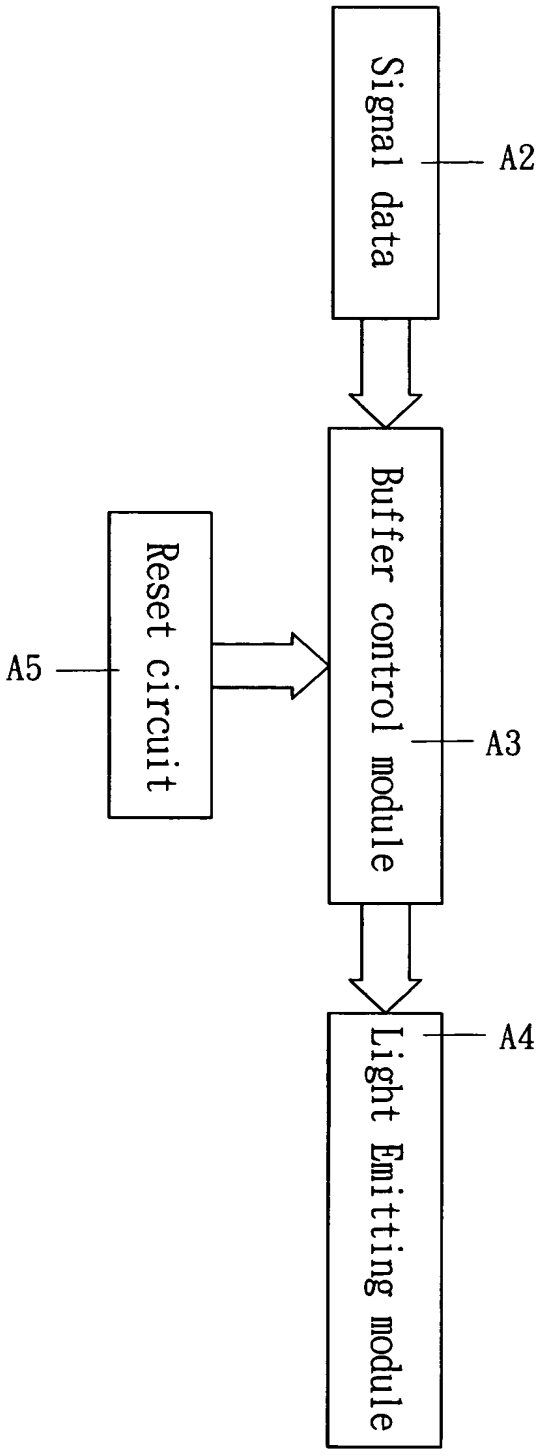


PRIOR ART
FIG. 1



PRIOR ART
FIG.2

	Low Speed	Full Speed	High Speed
D+	3.3V	0V	0.4V
D-	0V	3.3V	0.4V

FIG.3

Active/ Speed	Input			Output		
	Enable	D+	D-	Y1	Y2	Y3
NG	H	X	X	H	H	H
High	L	L	L	L	H	H
Full	L	H	L	H	L	H
Low	L	L	H	H	H	L

FIG.4

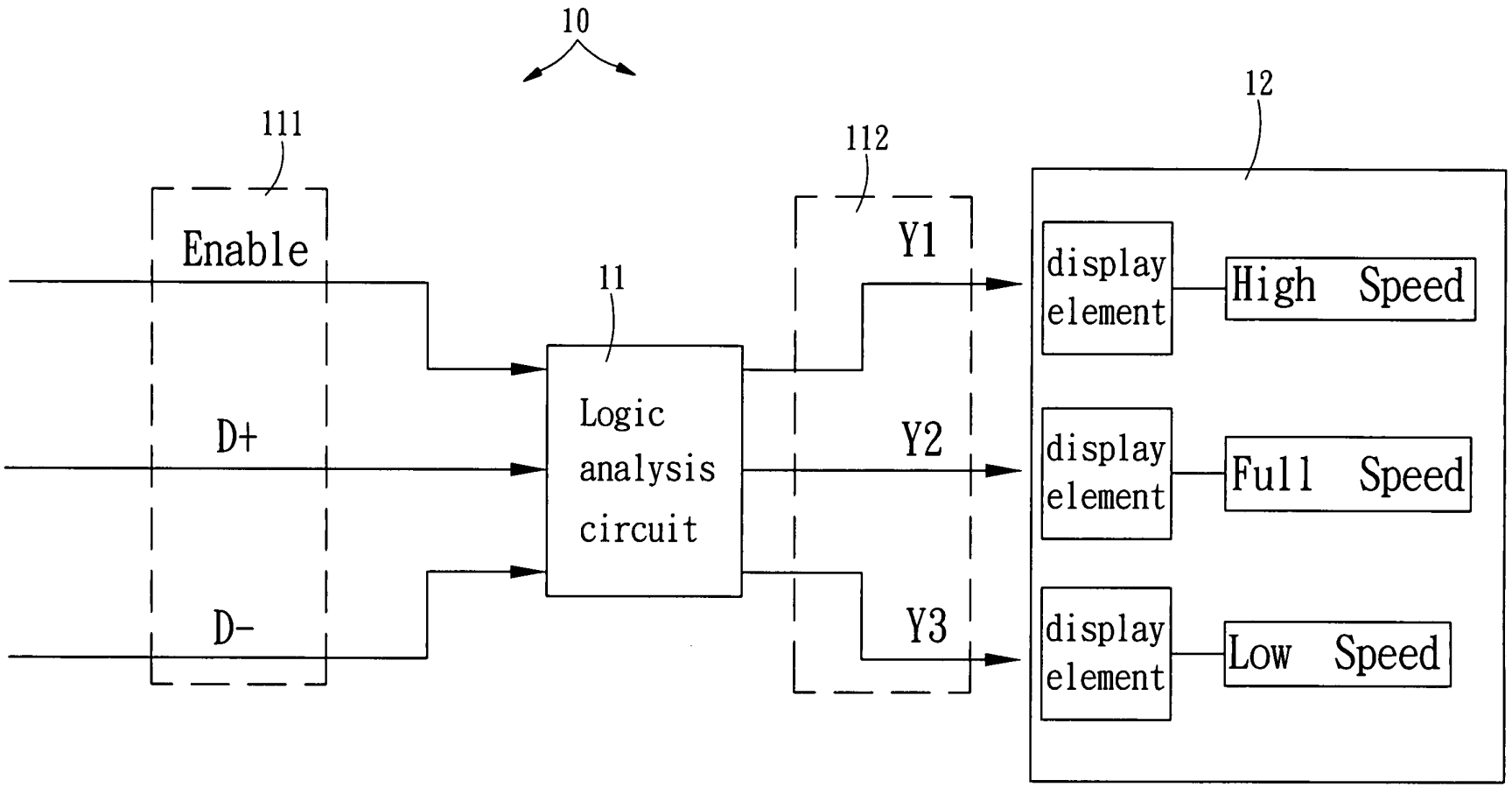

10
111
Enable
D+
D-
11
Logic
analysis
circuit
112
Y1
Y2
Y3
12
display
element
High Speed
display
element
Full Speed
display
element
Low Speed

FIG.5

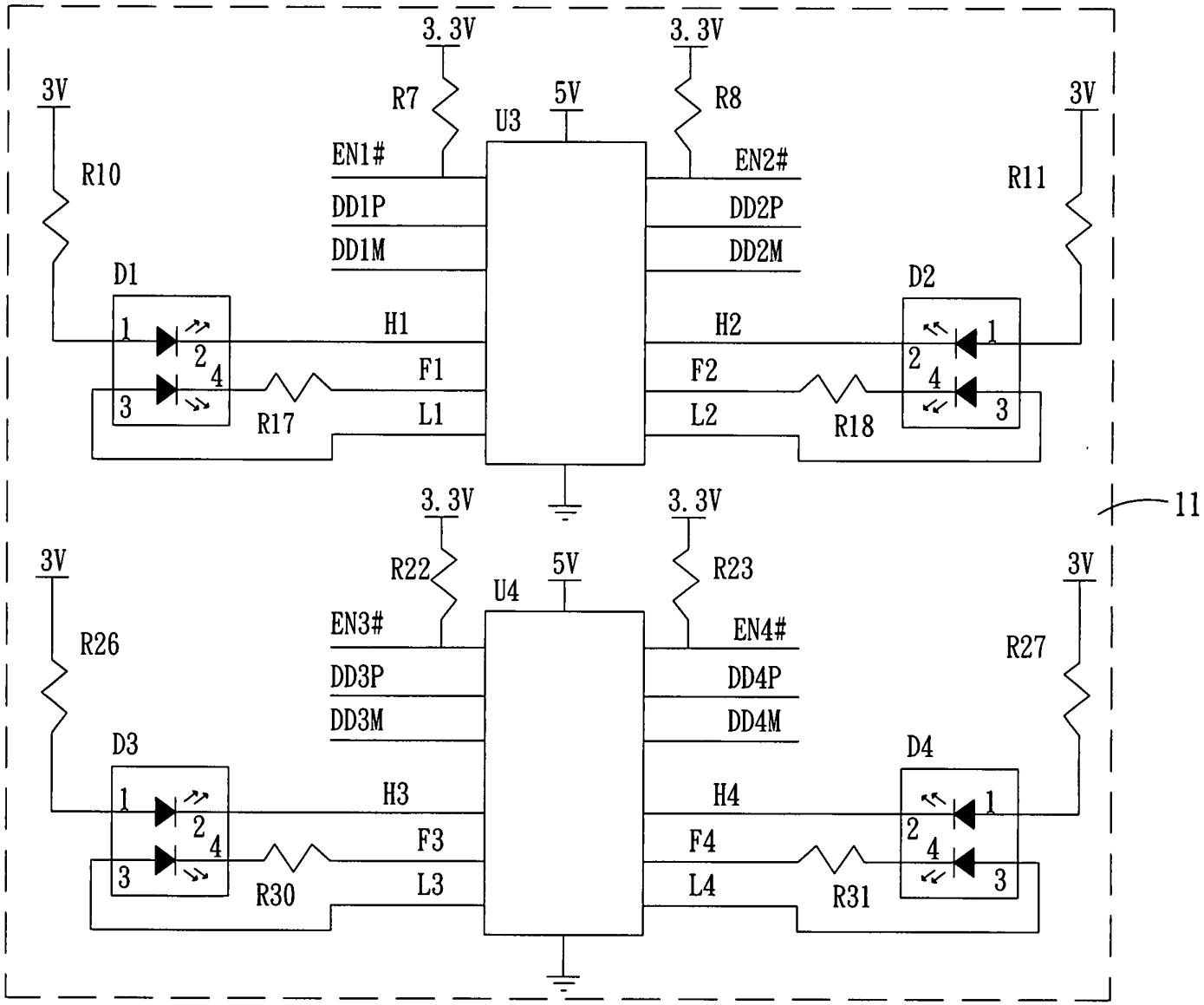

3.3V
3.3V
3V
R7
5V
R8
3V
U3
R10
EN1#
EN2#
R11
DD1P
DD2P
DD1M
DD2M
D1
D2
H1
H2
F1
F2
R17
L1
L2
R18
11
3.3V
3.3V
3V
R22
5V
R23
3V
U4
R26
EN3#
EN4#
R27
DD3P
DD4P
DD3M
DD4M
D3
D4
H3
H4
F3
F4
R30
L3
L4
R31

FIG.6

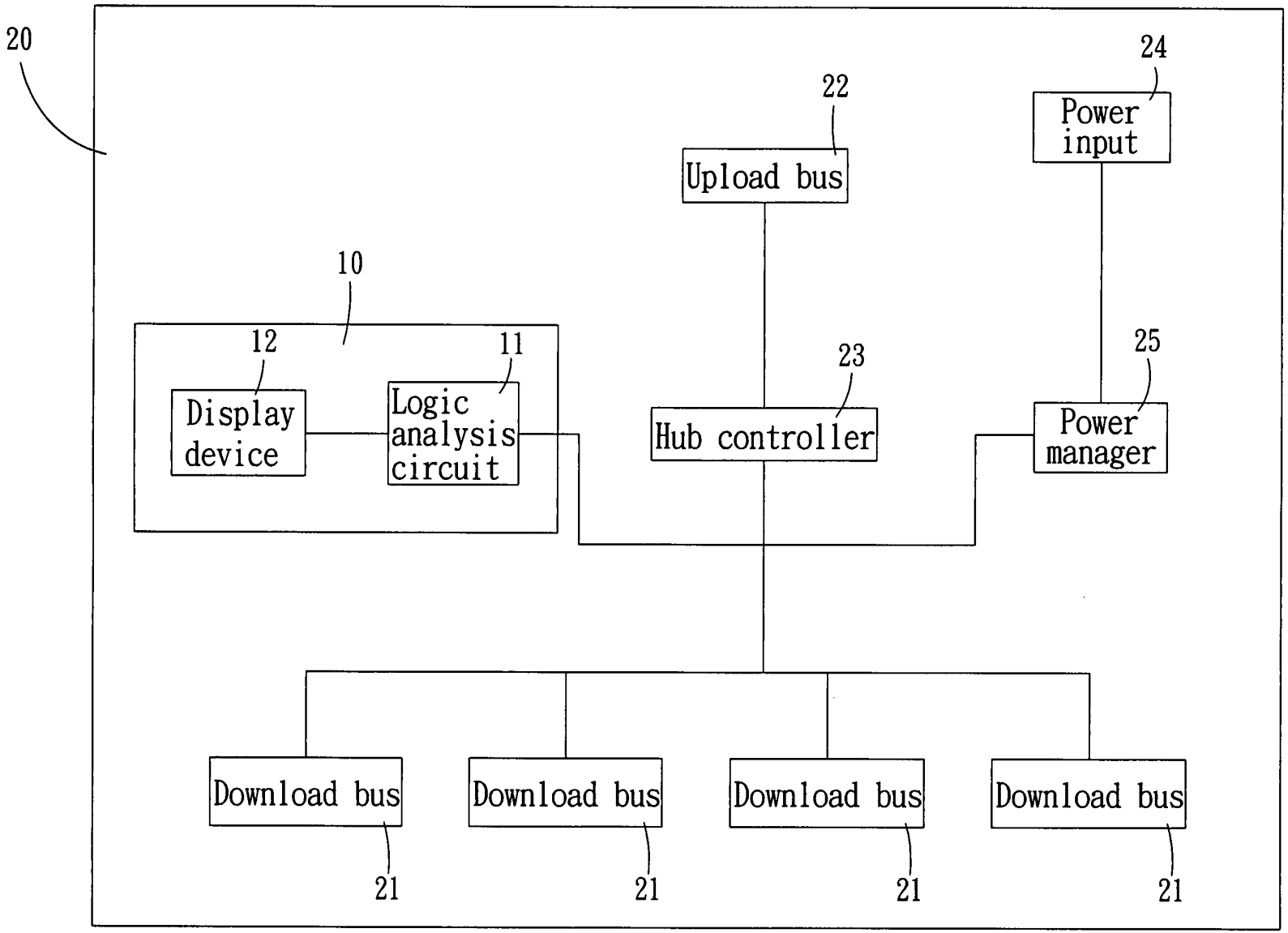

20
24
Power input
22
Upload bus
10
12
11
23
25
Display device
Logic analysis circuit
Hub controller
Power manager
Download bus
Download bus
Download bus
Download bus
21
21
21
21

FIG. 7

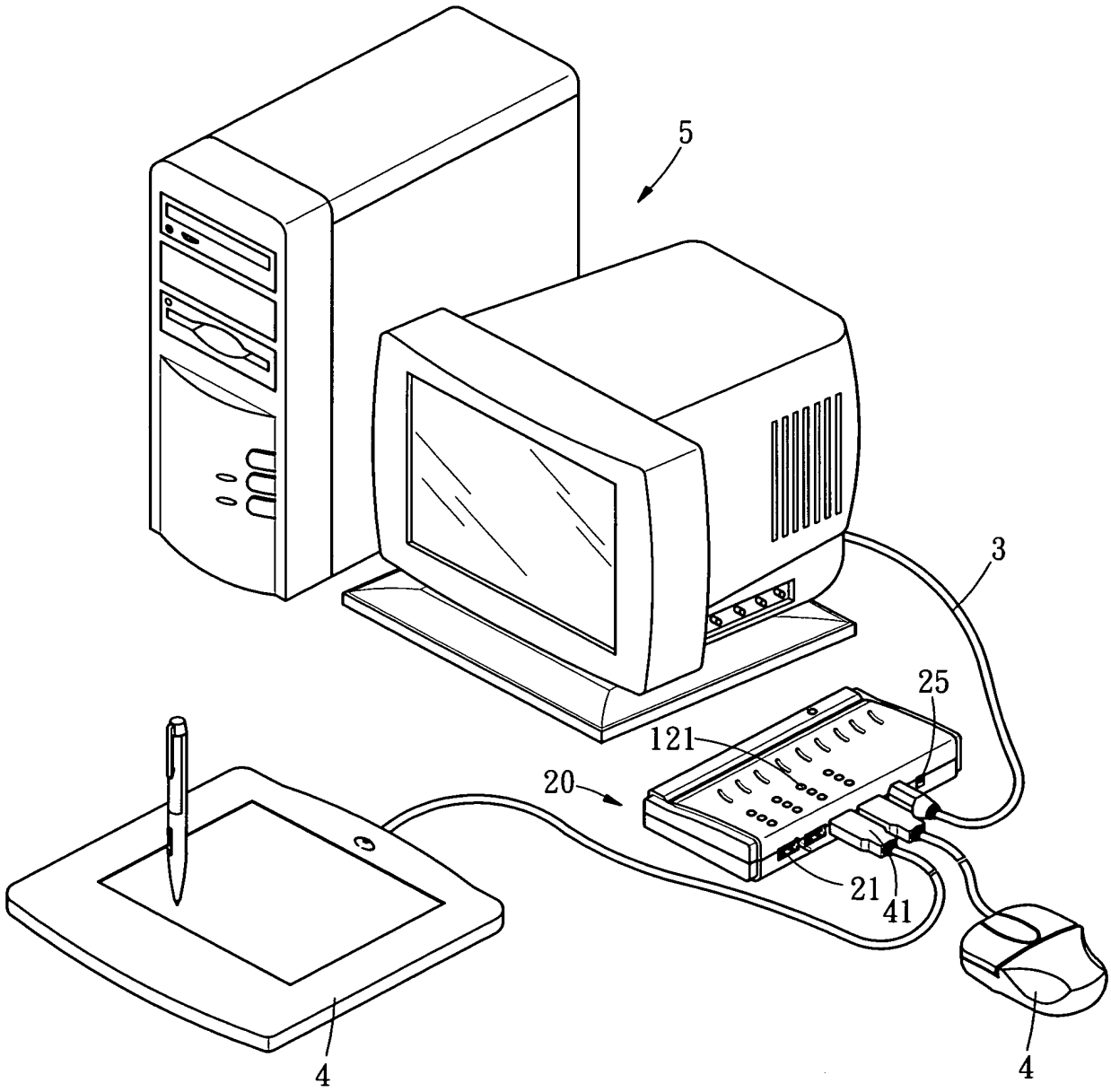


FIG.8

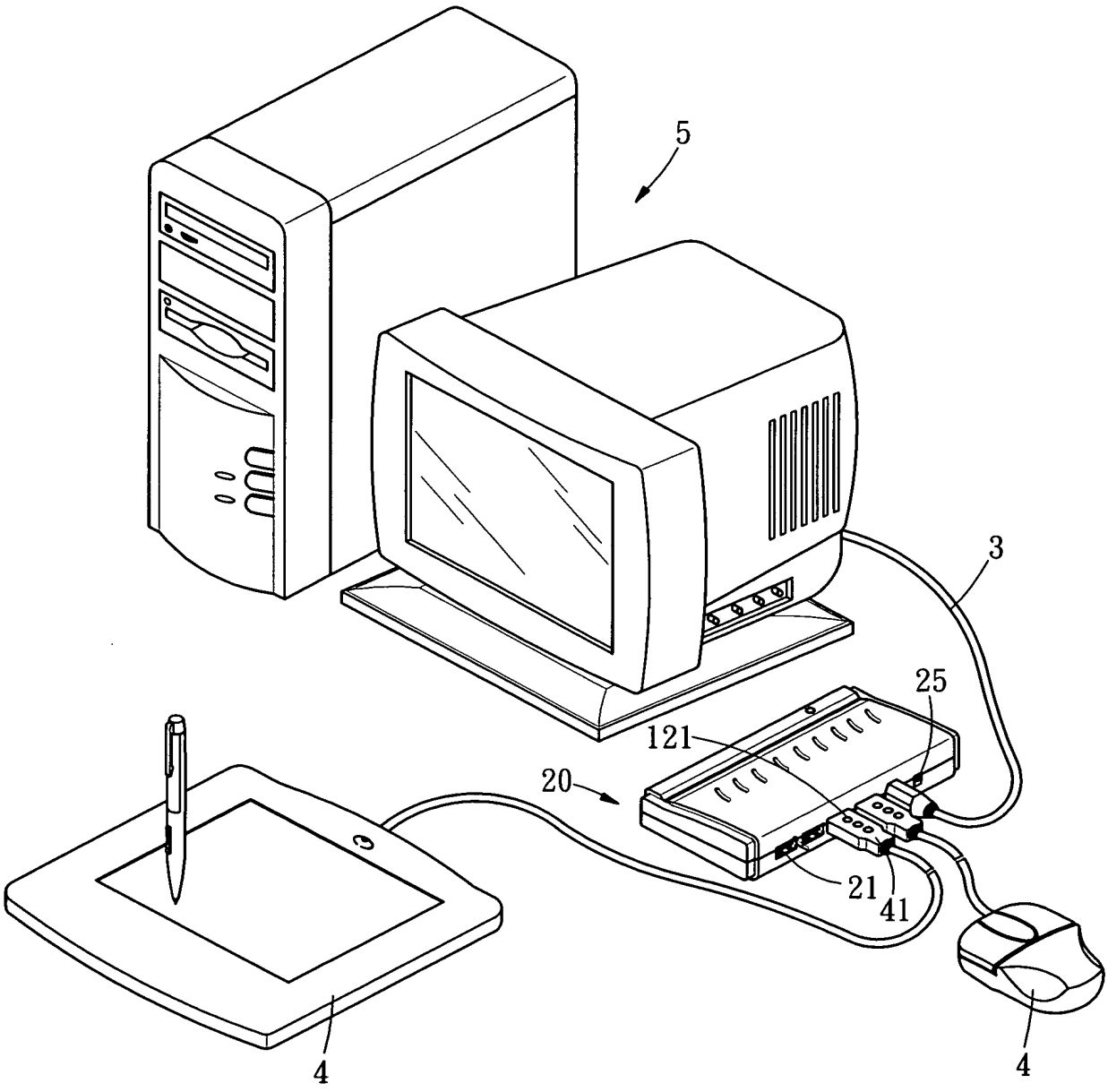


FIG. 9